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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,803	02/08/2001	Moinul I. Syed	A0312/7378 (RMA)	5583

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/779,803	SYED ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-6,30,32,33,36,39 and 41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,30,32,33,36,39 and 41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in respond to the Amendment filed on 12/8/2006, claims 1, 4-6, 30, 32-33, 36, 39, and 41 are pending in the Application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 6 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 6, the phrase "some" in line 7, renders the claim indefinite because it contains one, some, or all indiscriminately number or amount and unlimited or unmeasured quantity.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 30 and 41 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimizu (US PAT. 6,038,647).

Regarding claim 1, Shimizu discloses a cache memory system, i.e., multi-access cache memory device (1, figure 1) comprising an associative cache, i.e., four way associative (col. 6 lines 22-38), including a plurality of tag memory, i.e., tag array (2b, figure 1) locations for storing addresses, and a plurality of data memory location, i.e., data array (2a, figure 1) for storing data, the memory locations being organized as tow or more ways and each address presented to the associative cache being compared with the addresses stored in the tag memory locations in each of the two or more ways (col. 6 lines 22-37 and col. 11 line 66 through col. 12 line 9), and at least one controller, i.e., the switching mechanism control unit (5, figure 1) enables a first device, i.e., input port (3, figure 1) with address A, to access data memory location, without limitation as to data memory location, i.e., to access one of pair (2A, figure 1) in cache mechanism (2, figure 1), in a first way selected from the two or more ways, and enables a second device, i.e., second input port (3, figure 1) with address B, to access a data memory location, without limitation as to data memory location, in a second way selected from the two or more ways (col. 6 line 38 through col. 7 line 17), the first device accessing the data memory location in the first way and the second device being blocked from accessing the first way during access by the first device, the second device accessing the data memory location in the second way and the first device being blocked from accessing the second way during access by the second device, and the data memory locations in the first and second ways can be accessed concurrently by the first and second device, respectively, i.e., two or more access requests in parallel via the

plurality of input ports, the switching mechanism control unit, i.e., controller (5, figure 1) controls the state of switching of the switching mechanism so as to divide the plurality of pairs (2A, figure 1) into two or more non-overlapping subsets, i.e., one way blocking from another way, and subsequently supply access-data-specifying information, which accompanies each access request, to each of the relevant subsets, so as defined in figures 2(a)-6 with example of addresses A, B, and C which each has their respective way in each of the tag array (2b) and data array (2a), and (col. 4 lines 23-31, col. 6 line 39 through col. 7 line 17, col. 10 lines 25-45, and col. 17 lines 14-38).

Regarding claim 30, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 41, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 6, 36 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu (US PAT. 6,038,647) in view of Sakai (US PAT. 6,131,143).

Regarding claim 6, Shimizu discloses a cache memory system, i.e., multi-access cache memory device (1, figure 1) comprising an associative cache, i.e., four way associative (col. 6 lines 22-38), including a plurality of tag memory, i.e., tag array (2b, figure 1) locations for storing addresses, and a plurality of data memory location, i.e., data array (2a, figure 1) for storing data, the memory locations being organized as tow or more ways and each address presented to the associative cache being compared with the addresses stored in the tag memory locations in each of the two or more ways (col. 6 lines 22-37 and col. 11 line 66 through col. 12 line 9), and at least one controller, i.e., the switching mechanism control unit (5, figure 1) enables a first device, i.e., input port (3, figure 1) with address A, to access data memory location, without limitation as to data memory location, i.e., to access one of pair (2A, figure 1) in cache mechanism (2, figure 1), in a first way selected from the two or more ways, and enables a second device, i.e., second input port (3, figure 1) with address B, to access a data memory location, without limitation as to data memory location, in a second way selected from the two or more ways (col. 6 line 38 through col. 7 line 17), and the selected data from the data memory locations in the first and second ways being provided concurrently on respective ones of the plurality of cache output, so as defined in figures 2(a)-6 with example of addresses A, B, and C which each

has their respective way in each of the tag array (2b) and data array (2a), and (col. 4 lines 23-31, col. 6 line 39 through col. 7 line 17, col. 10 lines 25-45, and col. 17 lines 14-38). Shimizu differs from the claimed invention in not specifically teaches the cache memory system further comprising a plurality of cache outputs for providing data retrieved from the data memory locations, and first and second multiplexers having multiplexer inputs coupled to at lest some of the data memory locations, and multiplexer outputs coupled to the plurality of cache outputs. However, Sakai, in the analogous art, discloses a multi-way storage type cache memory system (figure 1) comprising a plurality of cache outputs i.e., output lines from 5a-5n, figure 1) for providing data retrieved from the memory locations (5a-5n, figure 1), a first multiplexer (6, figure 1) and a second multiplexer (7a-7n, figure 1) having multiplexer inputs coupled to at least some of the memory locations and multiplexer having multiplexer outputs coupled to the plurality of cache outputs via a way selector (9, figure 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the multi-access cache memory device of Shimizu comprising a plurality of cache outputs for providing data retrieved from the data memory locations, and first and second multiplexers having multiplexer inputs coupled to at lest some of the data memory locations, and multiplexer outputs coupled to the plurality of cache outputs, as per teaching by the multi-way storage type cache memory system of Sakai, because it decreases the power consumption and hit rate is maintained (col. 3 lines 38-40).

Regarding claim 36, the limitations of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 39, Sakai teaches at least one of the multiplexers (6 and 7a-7n, figure 1) to select one of the first and second addresses as its output while concurrently controlling another multiplexers to select the other of the first and second address as its output (col. 6 lines 20-32).

9. Claims 4-5 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu (US PAT. 6,038,647) in view of Liao et al. (US PAT. 6,857,061 hereinafter Liao).

Regarding claims 4-5, Shimizu teaches the first device comprising a processor (11, figure 19) configured and arranged to access the memory locations. Shimizu differs from the claimed invention in not specifically teaching the second device including a data transfer engine configured arranged to transfer data between the memory locations and a lower level memory, wherein the data transfer engine comprises a DMA controller. However, Liao, in the analogous art, teaches a microprocessor (10, figure 3) comprising a BIU/DMA (40, figure 3), read as a data transfer engine, configured and arranged to transfer data between the memory locations, i.e., cache line in L2 (36, figure 3) and a lower level memory (12, figure 3) in order to improve instruction format which may be used in connection with any suitable type of data processor, from microprocessor to supercomputers with a vector processing unit, thereby improving the operational efficiency (see Liao col. 4 lines 33-37). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the multi-access cache memory device of Shimizu including a data transfer engine configured arranged to transfer data between the memory locations and a lower level memory, wherein the data transfer engine comprises a DMA controller, as per teaching of Liao, in order to improve the operational efficiency.

Regarding claims 32-33, the limitations of the claims are rejected as the same reasons as set forth in claims 4-5.

Response to Arguments

10. Applicant's arguments with respect to claims 1, 4-6, 30, 32-33, 36-39 and 41 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Malamy et al. (US PAT. 5,675,765) discloses cache memory system with independently accessible subdivided cache tag arrays (abstract).

Arimilli et al. (US PAT. 6,023,746) discloses dual associative-cache directories allowing simultaneous read operation using two buses with multiplexers, address tags, memory block control signals, single clock cycle operation and error correction (abstract).

Steely et al. (US PAT. 5,509, 135) discloses multi-index multi-way set-associative cache (abstract).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on Mon - Fri 10:00am - 6:30pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Zhuo H. Li

Patent Examiner
February 22, 2007

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